1. (Previously Presented) A fin-type field effect transistor (FinFET) comprising:

a first fin having a central channel region and source and drain regions adjacent said channel region;

a gate structure intersecting said first fin and covering said channel region; and

a second fin consisting of a channel region, said second fin being parallel to said first fin and being covered by said gate structure, and said channel region of said second fin is devoid of a connection to any source or drain regions.

2. (Previously Presented) A fin-type field effect transistor (FinFET) comprising:

a first fin having a central channel region and source and drain regions adjacent said channel region;

a gate structure intersecting said first fin and covering said channel region; and

a second fin consisting of a channel region, said second fin being parallel to said first fin and being covered by said gate structure wherein said second fin has a length equal to a width of said gate structure.

3. (Previously Presented) A fin-type field effect transistor (FinFET) comprising:

a first fin having a central channel region and source and drain regions adjacent said channel region;

a gate structure intersecting said first fin and covering said channel region; and

a second fin consisting of a channel region, said second fin being parallel to said first fin and being covered by said gate structure, wherein said first fin is longer than said second fin.

4. (Previously Presented) The FinFET in claim 1, wherein said source and drain regions of said first fin extend beyond said gate structure.

5. (Previously Presented) A fin-type field effect transistor (FinFET) comprising:

a first fin having a central channel region and source and drain regions adjacent said channel region;

a gate structure intersecting said first fin and covering said channel region; and

a second fin consisting of a channel region, said second fin being parallel to said first fin and being covered by said gate structure, wherein said second fin does not extend beyond said gate structure.

6. (Previously Presented) The FinFET in claim 1, further comprising source and drain contacts covering said source and drain regions of said first fin.

7. (Previously Presented) The FinFET in claim 1, wherein no contacts are positioned adjacent said second fin.

8. (Previously Presented) A fin-type field effect transistor (FinFET) comprising:

a first fin having a central channel region and source and drain regions adjacent said channel region; and

a second fin consisting of a channel region, wherein said channel region of said second fin is devoid of a connection to any source or drain regions.

9. (Currently Amended) A fin-type field effect transistor (FinFET) comprising:

a first fin having a central channel region and source and drain regions adjacent said channel region; and

a second fin consisting of a ~~said~~ channel region, wherein said first fin is longer than said second fin.

10. (Currently Amended) The FinFET in claim 8, further comprising a gate intersecting said first fin and covering said channel region of said first fin.

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11. (Currently Amended) A fin-type field effect transistor (FinFET) comprising:

a first fin having a central channel region and source and drain regions adjacent said channel region; and

a second fin consisting of a ~~said~~ channel region, wherein said second fin has a length equal to a width of said gate structure.

12. (Previously Presented) The FinFET in claim 10, wherein said source and drain regions of said first fin extend beyond said gate structure.

13. (Currently Amended) A fin-type field effect transistor (FinFET) comprising:

a first fin having a central channel region and source and drain regions adjacent said channel region; and

a second fin consisting of a ~~said~~ channel region, wherein said second fin does not extend beyond said gate structure.

14. (Previously Presented) The FinFET in claim 8, further comprising source and drain contacts covering said source and drain regions of said first fin.

15. (Previously Presented) The FinFETs in claim 8, wherein no contacts are positioned adjacent said second fin.

16-29 (Cancelled).